REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1-11 stand rejected under obviousness-type double patenting based on various claims of U.S. Patent No. 6,194,762. In response to this rejection, all amended claims have been amended to recite an electrode which is connected to at least one of the pair of portions having n-type and p-type impurities. This obviates the double patenting rejection.

Claim 8 stands rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite. In response, claim 8 has been amended for definiteness herein.

Applicants call attention to the Information Disclosure Statement filed with the application on January 30, 2001. Copies of the cited documents were not provided in compliance with Rule 98(d). Please confirm that these references have been considered in this application by returning a copy of the forms with the Examiner's initials.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 11/20/01

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VERSION TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows:

1. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least a first thin film transistor and a second thin film transistor;

said first thin film transistor comprising:

a first semiconductor layer having first source and drain regions, a pair of lightly-doped regions and a first channel forming region therebetween;

a first gate electrode adjacent to said first channel forming region with a first gate insulating layer interposed therebetween, and

said second thin film transistor comprising:

a second semiconductor layer having second source and drain regions and a second channel forming region therebetween;

a second gate electrode adjacent to said second channel forming region with a second gate insulating layer interposed therebetween,

wherein said second channel forming region directly contacts with said second source and drain regions, [and]

wherein a pair portions containing n-type and p-type impurities are formed adjacent to said second source region and said second drain region[.], and

wherein an electrode is connected to at least one of said pair of portions.

2. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least a first thin film transistor and a second thin film transistor;

said first thin film transistor comprising:

a first semiconductor layer having first source and drain regions, a pair of lightly-doped regions and a first channel forming region therebetween;

a first gate electrode adjacent to said first channel forming region with a first gate insulating layer interposed therebetween, and

said second thin film transistor comprising:

a second semiconductor layer having second source and drain regions and a second channel forming region therebetween;

a second gate electrode adjacent to said second channel forming region with a second gate insulating layer interposed therebetween,

wherein said second source and drain regions contain p-type impurity and directly connect with said second channel forming region, [and]

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said second source region and said second drain region[.], and

wherein an electrode is connected to at least one of said pair of portions.

3. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least one thin film transistor, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said second source and drain regions, [and]

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region[.], and

wherein an electrode is connected to at least one of said pair of portions.

4. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least one thin film transistor, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said source and drain regions contain p-type impurity and directly connect with said channel forming region, [and]

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region[.], and

wherein an electrode is connected to at least one of said pair of portions.

8. (Amended) A semiconductor device having at least one thin film transistor formed over a substrate, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and

a channel forming region therebetween;

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said second source and drain regions, [and]

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region[.], and

wherein an electrode is connected to at least one of said pair of portions.

9. (Amended) A semiconductor device having at least one thin film transistor formed over a substrate, said thin film transistor comprising:

a semiconductor layer having a source and drain regions and a channel forming region therebetween;

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said source and drain regions contain p-type impurity and directly contact with said channel forming region, [and]

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain region[.],

wherein an electrode is connected to at least one of said pair of portions.